REMARKS

The rejection of claims 1 – 3, 5 and 6 under 35 USC 103(a) as being unpatentable over Booth, U.S. Patent No. 5,543,585 in view of applicant's admitted prior art, and Takeuchi, et al, U.S. Patent Application Publication 2001/0039891 is respectfully traversed.

The Examiner has acknowledged the Amendment filed by applicant on April 16, 2004 in which claims 1 and 7 were amended to make it clear that the plurality of bond pads are formed in the substrate and not on the substrate. In applicant's "REMARKS" this amendment to claim 1 was identified not only as an important feature of the subject invention but one which is not taught in Booth. To applicant's surprise, in the current Office Communication dated July 2, 2004, the Examiner has taken the position that forming the bond pads in the substrate was admitted by applicant to constitute prior art. Since this is not true, applicant has attempted, without success, to telephone the Examiner to arrange for a telephone interview on October 1, 2004 to discuss this allegation before expiration of the three month period for response in order to being this issue to the forefront. Applicant does not understand the basis upon which the Examiner has reached the conclusion that either Fig. 1 is prior art and/or that applicant has admitted that it is well known in the art to form bond pads in, i.e., internal to the substrate. Applicant has at no time indicated that Fig. 1A constitutes prior art. Moreover, there is nothing in the specification to suggest that Fig. 1A should be construed as prior art. Accordingly, the Examiner should forthwith discontinue referring to applicant's specification and/or figures as constituting prior art. Since the rejection is based on this assertion, applicant would like to discuss this with the Examiner in person or on the telephone. This would permit applicant to submit a supplemental response if the Office Action has been misconstrued.

It is also respectfully submitted that formation of the bond pads in (internal of) the substrate as claimed by applicant not only allows the conductive bumps to form flatly on the substrate. i.e., permits the top surface of the first encapsulant to be formed

in coplanar alignment with the flat end of the conductive elements as set forth in claim 1. This also shortens the distance between the chip and the substrate making the entire package more compact in size. These benefits are attributable to formation of the bond pads when formed internal of the substrate and are clearly not obvious to one of ordinary skill in the art.

If the Examiner otherwise considers forming the plurality of bond pads "in the substrate" as opposed to "on the substrate" to be an obvious matter of design choice, applicant would like prior art to be cited by the Examiner which technically supports this conclusion. Once again, if the allegation of the Examiner is based on admitted prior art applicant refutes this allegation as unfounded. The Examiner is not free to make assumptions from the specification as to what constitutes prior art. There must be positive teaching by applicant or an express admission of prior art.

On page 2 of the Office Action the Examiner admits that Booth does not teach or suggest forming the bond pads in the substrate, i.e., internal of the substrate. Furthermore, it is evident from Booth that the conductive pads 8 are formed over, i.e., on the substrate 1 before the conductive adhesive bumps or pegs 4 are applied by mask screening onto the conductive pads 8. By forming the conductive pads 8 over the substrate 1 the conductive adhesive bumps or pegs 4 will not lie properly on the same plane due to a step difference created by the conductive pads on the substrate permitting misalignment to occur during the mask printing operation. For this reason, the packaging process disclosed by Booth, et al has less tolerance for misalignment relative to that of the subject invention.

The Examiner has also alleged that "applicant's admitted prior art teaches that it is well known in the art to encapsulate a chip and to implant solder balls to the opposite side of the substrate". The Examiner refers to applicant's specification on page 1, third paragraph. Is the Examiner interpreting the third paragraph on page 1 of the specification as a teaching of forming conductive pads in (internal of) the substrate? Does this support a teaching of a coplanar surface between the subsequently formed first encapsulant and conductive bumps as claimed in claim 1 of applicant's application?

The allegation of the Examiner's that "applicant's admitted prior art teaches that it is well known to form the bond pads in the substrate" is simply not true. Since this is integral to the rejection of the claims, applicant would like to have an interview with the Examiner to resolve this issue. It must follow that without the allegation of what applicant alleges to be prior art, the Examiner would be willing to withdraw the rejection of claim 1.

Claims 2 – 6 are dependent claims which depend from claim 1 and are believed patentable for the same reasons as given heretofore.

The rejection of claim 7 as being obvious in view of Booth, U.S. Patent No. 5,543,585 applicant's admitted prior art, Takeuchi, et al, U.S. Patent Application Publication 2001/0039891 and further in view of Cook, U.S. Patent No. 6,331,446 is respectfully traversed.

Claim 7 is a dependent claim which should also be patentable for the same reasons as given heretofore in connection with claim 1. However, in addition, it is clearly disclosed in Cook, et al '446 that the encapsulant alleged by the Examiner is an underfill material (26) used to enclose and seal the other underfill material (24). As is understood by one skilled in the pertinent art underfill material is used in the underfill process for filling up the gap between two layers. Accordingly, the encapsulant that is formed by the molding process in applicant's invention is clearly different from the need for underfill material using the underfill process taught in Cook. Applicant has explained on many instances that voids and gap formations associated with the underfill process is avoided using the method of the subject invention.

The rejection of claim 8 under 35 USC 103(a) as being obvious based upon Booth '585 in view of applicant's admitted prior art, Takeuchi, et al, U.S. Patent Application Publication No. 2001/0039891 and further in view of Lai, U.S. Patent No. 6,323,066 is respectfully traversed.

Claim 8 is a dependent claim which is believed to be patentable for the same reasons as given heretofore.

U.S. Patent No.6,323,066 is directed to a heat sink which is attached to the substrate and over the chip and then encapsulating the heat. There is nothing in Lai, et al which would teach or suggest forming conductive pads in (internal of) the substrate or forming the conductive bumps in such a manner that the flat ends of the conductive bumps will be exposed and level with the top surface of the subsequently formed first encapsulant.

For all of the foregoing reasons applicant believes that the rejection of claims 1 – 3 and 6 – 8 should be withdrawn.

Reconsideration and allowance of claims 1 – 3 and 6 – 8 is respectfully solicited.

Respectfully submitted,

Eugene Lieberstein
Reg. No. 24,645

ANDERSON, KILL & OLICK
1251 Avenue of the Americas
New York, New York 10020-1182
(212) 278-1000

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 4, 2004.

Mary Washburn

Date: October 4 2004